Register code HCS12

mc9s12dp512.h

.h header file

```
#ifndef _MC9S12DP512_H
#define _MC9S12DP512_H

/*****************************************************************************
*     Filename  : mc9s12dp512.h
*     Processor : MC9S12DP512
*     DocumentId: 9S12DP512DGV1/D
*     Version   : V01.20
*     Date      : 14-Jan-2003
*     Abstract  :
*         This implements an IO devices mapping.
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*     mail      : info@chipwerks.com
*****************************************************************************

                MC9S12DP512 USER CONFIGURABLE MEMORY MAP

Assuming that a '0' was driven onto port K bit 7 during MCU
is reset into normal expanded wide or narrow mode.

0x0000 - 0x03FF : Registers , Mappable to any 2K Boundary with in first 32K.
0x0000 - 0x0FFF : 4K Bytes EEPROM(Mappable to any 4K block)
0x0800 - 0x3FFF : 14K Bytes of RAM (Mappable to any 16K and alignable to top or
0x4000 - 0x7FFF : 16K Fixed Flash Page 0x3e = 62 (This is dependant on the state
0x8000 - 0xBFFF : 16K Page window 32*16K Flash EEPROM pages
0xC000 - 0xFFFF : 16K Fixed Flash Page 0x3f = 63
0xFF00 - 0xFFFF : BDM (If active) for Special Single Chip.

*****************************************************************************

                    MC9S12DP512 DEVICE MEMORY MAP OVER VIEW

Address                         Module                          (Bytes)Size
-----------------------------------------------------------------------------
$0000 - $000F       HCS12 Multiplexed External Bus Interface            16
$0010 - $0014       HCS12 Module Mapping Control                         5
$0015 - $0016       HCS12 Interrupt                                      2
$0017 - $0019       Reserved                                             3
$001A - $001B       Device ID register (PARTID)                          2
$001C - $001D       HCS12 Module Mapping Control                         2
$001E               HCS12 Multiplexed External Bus Interface             1
$001F               HCS12 Interrupt                                      1
$0020 - $0027       Reserved                                             8
$0028 - $002F       HCS12 Breakpoint                                     8
$0030 - $0031       HCS12 Module Mapping Control                         2
$0032 - $0033       HCS12 Multiplexed External Bus Interface             2
$0034 - $003F       Clock and Reset Generator (PLL, RTI, COP)           12
$0040 - $007F       Enhanced Capture Timer 16-bit 8 channels            64
$0080 - $009F       Analog to Digital Converter 10-bit 8 channels (ATD0)  32
$00A0 - $00C7       Pulse Width Modulator 8-bit 8 channels (PWM)        40
$00C8 - $00CF       Serial Communications Interface 0 (SCI0)             8
$00D0 - $00D7       Serial Communications Interface 0 (SCI1)             8
$00D8 - $00DF       Serial Peripheral Interface (SPI0)                   8
$00E0 - $00E7       Inter IC Bus                                         8
$00E8 - $00EF       Byte Data Link Controller (BDLC)                     8
$00F0 - $00F7       Serial Peripheral Interface (SPI1)                   8
$00F8 - $00FF       Serial Peripheral Interface (SPI2)                   8
$0100 - $010F       Flash Control Register                              16
$0110 - $011B       EEPROM Control Register                             12
```

```
 61: $011C - $011F       Reserved                                                4
 62: $0120 - $013F       Analog to Digital Converter 10-bit 8 channels (ATD1)   32
 63: $0140 - $017F       Motorola Scalable Can (CAN0)                           64
 64: $0180 - $01BF       Motorola Scalable Can (CAN1)                           64
 65: $01C0 - $01FF       Motorola Scalable Can (CAN2)                           64
 66: $0200 - $023F       Motorola Scalable Can (CAN3)                           64
 67: $0240 - $027F       Port Integration Module (PIM)                          64
 68: $0280 - $02BF       Motorola Scalable Can (CAN4)                           64
 69: $02C0 - $03FF       Reserved                                              320
 70: $0000 - $0FFF       EEPROM array                                         4096
 71: $0800 - $3FFF       RAM array                                           14336
 72: $4000 - $7FFF       Fixed Flash EEPROM array
 73:                     incl. 1K, 2K, 4K or 8K Protected Sector at start    16384
 74:
 75:
 76: $8000 - $BFFF       Flash EEPROM Page Window                            16384
 77: $C000 - $FFFF       Fixed Flash EEPROM array
 78:                     incl. 2K, 4K, 8K or 16K Protected Sector at end
 79:                     and 256 bytes of Vector Space at $FF80 - $FFFF      16384
 80:
 81: /*****************************************************************************/
 82:
 83:
 84: #define _REG_BASE        0
 85: #define _ADDR(off)      (unsigned char volatile *)(_REG_BASE + off)
 86: #define _P(off)         *(unsigned char volatile *)(_REG_BASE + off)
 87: #define _LP(off)        *(unsigned short volatile *)(_REG_BASE + off)
 88:
 89:
 90: #define  PORTA   _P(0x00)
 91: #define  PORTAB   _LP(0x00)
 92: #define  PORTB   _P(0x01)
 93: #define  DDRA   _P(0x02)
 94: #define  DDRAB   _LP(0x02)
 95: #define  DDRB   _P(0x03)
 96:
 97: //#define  Reserved   _P(0x04)
 98: //#define  Reserved   _P(0x05)
 99: //#define  Reserved   _P(0x06)
100: //#define  Reserved   _P(0x07)
101:
102: #define  PORTE   _P(0x08)
103: #define  DDRE   _P(0x09)
104: #define  PEAR   _P(0x0A)
105: #define  MODE   _P(0x0B)
106: #define  PUCR   _P(0x0C)
107: #define  RDRIV   _P(0x0D)
108: #define  EBICTL   _P(0x0E)
109: //#define  Reserved   _P(0x0F)
110:
111:
112: #define  INITRM   _P(0x10)
113: #define  INITRG   _P(0x11)
114: #define  INITEE   _P(0x12)
115: #define  MISC   _P(0x13)
116: //#define  Reserved   _P(0x14)
117:
118:
119: #define  ITCR   _P(0x15)
120: #define  ITEST   _P(0x16)
```

```
121:
122:
123: //#define  Reserved   _P(0x17)
124: //#define  Reserved   _P(0x18)
125: //#define  Reserved   _P(0x19)
126:
127:
128: #define  PARTIDH   _P(0x1A)
129: #define  PARTIDL   _P(0x1B)
130:
131:
132: #define  MEMSIZ0   _P(0x1C)
133: #define  MEMSIZ1   _P(0x1D)
134:
135:
136: #define  INTCR   _P(0x1E)
137:
138:
139: #define  HPRIO   _P(0x1F)
140:
141:
142: //#define  Reserved   _P(0x20)
143: //#define  Reserved   _P(0x21)
144: //#define  Reserved   _P(0x22)
145: //#define  Reserved   _P(0x23)
146: //#define  Reserved   _P(0x24)
147: //#define  Reserved   _P(0x25)
148: //#define  Reserved   _P(0x26)
149: //#define  Reserved   _P(0x27)
150:
151:
152: #define  BKPCT0   _P(0x28)
153: #define  BKPCT1   _P(0x29)
154: #define  BKP0X   _P(0x2A)
155: #define  BKP0H   _P(0x2B)
156: #define  BKP0L   _P(0x2C)
157: #define  BKP1X   _P(0x2D)
158: #define  BKP1H   _P(0x2E)
159: #define  BKP1L   _P(0x2F)
160:
161:
162: #define  PPAGE   _P(0x30)
163: //#define  Reserved   _P(0x31)
164:
165:
166: #define  PORTK   _P(0x32)
167: #define  DDRK   _P(0x33)
168:
169:
170: #define  SYNR   _P(0x34)
171: #define  REFDV   _P(0x35)
172: #define  CRGFLG   _P(0x37)
173: #define  CRGINT   _P(0x38)
174: #define  CLKSEL   _P(0x39)
175: #define  PLLCTL   _P(0x3A)
176: #define  RTICTL   _P(0x3B)
177: #define  COPCTL   _P(0x3C)
178: #define  FORBYP   _P(0x3D)
179: #define  CTCTL    _P(0x3E)
180: #define  ARMCOP   _P(0x3F)
```

```
181:
182:
183: #define  TIOS   _P(0x40)
184: #define  CFORC   _P(0x41)
185: #define  OC7M   _P(0x42)
186: #define  OC7D   _P(0x43)
187: #define  TCNT   _LP(0x44)
188: #define  TCNTHi   _P(0x44)
189: #define  TCNTLo   _P(0x45)
190: #define  TSCR1   _P(0x46)
191: #define  TTOV   _P(0x47)
192: #define  TCTL1   _P(0x48)
193: #define  TCTL2   _P(0x49)
194: #define  TCTL3   _P(0x4A)
195: #define  TCTL4   _P(0x4B)
196: #define  TIE   _P(0x4C)
197: #define  TSCR2   _P(0x4D)
198: #define  TFLG1   _P(0x4E)
199: #define  TFLG2   _P(0x4F)
200: #define  TC0   _LP(0x50)
201: #define  TC0Hi   _P(0x50)
202: #define  TC0Lo   _P(0x51)
203: #define  TC1   _LP(0x52)
204: #define  TC1Hi   _P(0x52)
205: #define  TC1Lo   _P(0x53)
206: #define  TC2   _LP(0x54)
207: #define  TC2Hi   _P(0x54)
208: #define  TC2Lo   _P(0x55)
209: #define  TC3   _LP(0x56)
210: #define  TC3Hi   _P(0x56)
211: #define  TC3Lo   _P(0x57)
212: #define  TC4   _LP(0x58)
213: #define  TC4Hi   _P(0x58)
214: #define  TC4Lo   _P(0x59)
215: #define  TC5   _LP(0x5A)
216: #define  TC5Hi   _P(0x5A)
217: #define  TC5Lo   _P(0x5B)
218: #define  TC6   _LP(0x5C)
219: #define  TC6Hi   _P(0x5C)
220: #define  TC6Lo   _P(0x5D)
221: #define  TC7   _LP(0x5E)
222: #define  TC7Hi   _P(0x5E)
223: #define  TC7Lo   _P(0x5F)
224: #define  PACTL   _P(0x60)
225: #define  PAFLG   _P(0x61)
226: #define  PACN3   _P(0x62)
227: #define  PACN32   _LP(0x62)
228: #define  PACN2   _P(0x63)
229: #define  PACN1   _P(0x64)
230: #define  PACN10   _LP(0x64)
231: #define  PACN0   _P(0x65)
232: #define  MCCTL   _P(0x66)
233: #define  MCFLG   _P(0x67)
234: #define  ICPAR   _P(0x68)
235: #define  DLYCT   _P(0x69)
236: #define  ICOVW   _P(0x6A)
237: #define  ICSYS   _P(0x6B)
238: //#define  Reserved   _P(0x6C)
239: #define  TIMTST  _P(0x6D)
240: //#define  Reserved   _P(0x6E)
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```
241: //#define  Reserved   _P(0x6F)
242: #define  PBCTL   _P(0x70)
243: #define  PBFLG   _P(0x71)
244: #define  PA32H   _LP(0x72)
245: #define  PA3H   _P(0x72)
246: #define  PA2H   _P(0x73)
247: #define  PA10H   _LP(0x74)
248: #define  PA1H   _P(0x74)
249: #define  PA0H   _P(0x75)
250: #define  MCCNT   _LP(0x76)
251: #define  MCCNThi   _P(0x76)
252: #define  MCCNTlo   _P(0x77)
253: #define  TC0H   _LP(0x78)
254: #define  TC0Hhi   _P(0x78)
255: #define  TC0Hlo   _P(0x79)
256: #define  TC1H   _LP(0x7A)
257: #define  TC1Hhi   _P(0x7A)
258: #define  TC1Hlo   _P(0x7B)
259: #define  TC2H   _LP(0x7C)
260: #define  TC2Hhi   _P(0x7C)
261: #define  TC2Hlo   _P(0x7D)
262: #define  TC3H   _LP(0x7E)
263: #define  TC3Hhi   _P(0x7E)
264: #define  TC3Hlo   _P(0x7F)
265:
266:
267: #define  ATD0CTL0   _P(0x80)
268: #define  ATD0CTL01   _LP(0x80)
269: #define  ATD0CTL1   _P(0x81)
270: #define  ATD0CTL2   _P(0x82)
271: #define  ATD0CTL23   _LP(0x82)
272: #define  ATD0CTL3   _P(0x83)
273: #define  ATD0CTL4   _P(0x84)
274: #define  ATD0CTL45   _LP(0x84)
275: #define  ATD0CTL5   _P(0x85)
276: #define  ATD0STAT0   _P(0x86)
277: //#define  Reserved   _P(0x87)
278: #define  ATD0TEST0   _P(0x88)
279: #define  ATD0TEST1   _P(0x89)
280: //#define  Reserved  _P(0x8A)
281: #define  ATD0STAT1   _P(0x8B)
282: //#define  Reserved  _P(0x8c)
283: #define  ATD0DIEN   _P(0x8D)
284: //#define  Reserved  _P(0x8E)
285: #define  PORTAD0   _P(0x8F)
286: #define  ATD0DR0   _LP(0x90)
287: #define  ATD0DR0H   _P(0x90)
288: #define  ATD0DR0L   _P(0x91)
289: #define  ATD0DR1   _LP(0x92)
290: #define  ATD0DR1H   _P(0x92)
291: #define  ATD0DR1L   _P(0x93)
292: #define  ATD0DR2   _LP(0x94)
293: #define  ATD0DR2H   _P(0x94)
294: #define  ATD0DR2L   _P(0x95)
295: #define  ATD0DR3   _LP(0x96)
296: #define  ATD0DR3H   _P(0x96)
297: #define  ATD0DR3L   _P(0x97)
298: #define  ATD0DR4   _LP(0x98)
299: #define  ATD0DR4H   _P(0x98)
300: #define  ATD0DR4L   _P(0x99)
```

```
301: #define  ATD0DR5   _LP(0x9A)
302: #define  ATD0DR5H   _P(0x9A)
303: #define  ATD0DR5L   _P(0x9B)
304: #define  ATD0DR6   _LP(0x9C)
305: #define  ATD0DR6H   _P(0x9C)
306: #define  ATD0DR6L   _P(0x9D)
307: #define  ATD0DR7   _LP(0x9E)
308: #define  ATD0DR7H   _P(0x9E)
309: #define  ATD0DR7L   _P(0x9F)
310:
311:
312: #define  PWME   _P(0xA0)
313: #define  PWMPOL   _P(0xA1)
314: #define  PWMCLK   _P(0xA2)
315: #define  PWMPRCLK   _P(0xA3)
316: #define  PWMCAE   _P(0xA4)
317: #define  PWMCTL   _P(0xA5)
318: #define  PWMTST   _P(0xA6)
319: #define  PWMPRSC   _P(0xA7)
320: #define  PWMSCLA   _P(0xA8)
321: #define  PWMSCLB   _P(0xA9)
322: #define  PWMSCNTA   _P(0xAA)
323: #define  PWMSCNTAB   _LP(0xAA)
324: #define  PWMSCNTB   _P(0xAB)
325: #define  PWMCNT0   _P(0xAC)
326: #define  PWMCNT01   _LP(0xAC)
327: #define  PWMCNT1   _P(0xAD)
328: #define  PWMCNT2   _P(0xAE)
329: #define  PWMCNT23   _LP(0xAE)
330: #define  PWMCNT3   _P(0xAF)
331: #define  PWMCNT4   _P(0xB0)
332: #define  PWMCNT45   _LP(0xB0)
333: #define  PWMCNT5   _P(0xB1)
334: #define  PWMCNT6   _P(0xB2)
335: #define  PWMCNT67   _LP(0xB2)
336: #define  PWMCNT7   _P(0xB3)
337: #define  PWMPER0   _P(0xB4)
338: #define  PWMPER01   _LP(0xB4)
339: #define  PWMPER1   _P(0xB5)
340: #define  PWMPER2   _P(0xB6)
341: #define  PWMPER23   _LP(0xB6)
342: #define  PWMPER3   _P(0xB7)
343: #define  PWMPER4   _P(0xB8)
344: #define  PWMPER45   _LP(0xB8)
345: #define  PWMPER5   _P(0xB9)
346: #define  PWMPER6   _P(0xBA)
347: #define  PWMPER67   _LP(0xBA)
348: #define  PWMPER7   _P(0xBB)
349: #define  PWMDTY0   _P(0xBC)
350: #define  PWMDTY01   _LP(0xBC)
351: #define  PWMDTY0   _P(0xBC)
352: #define  PWMDTY1   _P(0xBD)
353: #define  PWMDTY2   _P(0xBE)
354: #define  PWMDTY23   _LP(0xBE)
355: #define  PWMDTY3   _P(0xBF)
356: #define  PWMDTY4   _P(0xC0)
357: #define  PWMDTY45   _LP(0xC0)
358: #define  PWMDTY5   _P(0xC1)
359: #define  PWMDTY6   _P(0xC2)
360: #define  PWMDTY67   _LP(0xC2)
```

```
361: #define  PWMDTY7   _P(0xC3)
362: #define  PWMSDN   _P(0xC4)
363: //#define  Reserved   _P(0xC5)
364: //#define  Reserved   _P(0xC6)
365: //#define  Reserved   _P(0xC7)
366:
367:
368: #define  SCI0BD   _LP(0xC8)
369: #define  SCI0BDH   _P(0xC8)
370: #define  SCI0BDL   _P(0xC9)
371: #define  SCI0CR12   _LP(0xCA)
372: #define  SCI0CR1   _P(0xCA)
373: #define  SCI0CR2   _P(0xCB)
374: #define  SCI0SR12   _LP(0xCC)
375: #define  SCI0SR1   _P(0xCC)
376: #define  SCI0SR2   _P(0xCD)
377: #define  SCI0DR    _LP(0xCE)
378: #define  SCI0DRH   _P(0xCE)
379: #define  SCI0DRL   _P(0xCF)
380:
381:
382: #define  SCI1BD   _LP(0xD0)
383: #define  SCI1BDH   _P(0xD0)
384: #define  SCI1BDL   _P(0xD1)
385: #define  SCI1CR12   _LP(0xD2)
386: #define  SCI1CR1   _P(0xD2)
387: #define  SCI1CR2   _P(0xD3)
388: #define  SCI1SR12   _LP(0xD4)
389: #define  SCI1SR1   _P(0xD4)
390: #define  SCI1SR2   _P(0xD5)
391: #define  SCI1DR   _LP(0xD6)
392: #define  SCI1DRH   _P(0xD6)
393: #define  SCI1DRL   _P(0xD7)
394:
395:
396: #define  SPI0CR12   _LP(0xD8)
397: #define  SPI0CR1   _P(0xD8)
398: #define  SPI0CR2   _P(0xD9)
399: #define  SPI0BR   _P(0xDA)
400: #define  SPI0SR   _P(0xDB)
401: //#define  Reserved   _P(0xDC)
402: #define  SPI0DR   _P(0xDD)
403: //#define  Reserved   _P(0xDE)
404: //#define  Reserved   _P(0xDF)
405:
406:
407: #define  IBAD   _P(0xE0)
408: #define  IBFD   _P(0xE1)
409: #define  IBCR   _P(0xE2)
410: #define  IBSR   _P(0xE3)
411: #define  IBDR   _P(0xE4)
412: //#define  Reserved   _P(0xE5)
413: //#define  Reserved   _P(0xE6)
414: //#define  Reserved   _P(0xE7)
415:
416:
417: #define  DLCBCR1   _P(0xE8)
418: #define  DLCBSVR   _P(0xE9)
419: #define  DLCBCR2   _P(0xEA)
420: #define  DLCBDR   _P(0xEB)
```

```
421: #define  DLCBARD   _P(0xEC)
422: #define  DLCBRSR   _P(0xED)
423: #define  DLCSCR   _P(0xEE)
424: #define  DLCBSTAT   _P(0xEF)
425:
426:
427: #define  SPI1CR12   _LP(0xF0)
428: #define  SPI1CR1   _P(0xF0)
429: #define  SPI1CR2   _P(0xF1)
430: #define  SPI1BR   _P(0xF2)
431: #define  SPI1SR   _P(0xF3)
432: //#define  Reserved   _P(0xF4)
433: #define  SPI1DR   _P(0xF5)
434: //#define  Reserved   _P(0xF6)
435: //#define  Reserved   _P(0xF7)
436:
437:
438: #define  SPI2CR12   _LP(0xF8)
439: #define  SPI2CR1   _P(0xF8)
440: #define  SPI2CR2   _P(0xF9)
441: #define  SPI2BR   _P(0xFA)
442: #define  SPI2SR   _P(0xFB)
443: //#define  Reserved   _P(0xFC)
444: #define  SPI2DR   _P(0xFD)
445: //#define  Reserved   _P(0xFE)
446: //#define  Reserved   _P(0xFF)
447:
448:
449:
450: #define  FCLKDIV   _P(0x100)
451: #define  FSEC   _P(0x101)
452: #define  FTSTMOD  _P(0x102)
453: #define  FCNFG   _P(0x103)
454: #define  FPROT   _P(0x104)
455: #define  FSTAT   _P(0x105)
456: #define  FCMD   _P(0x106)
457: //#define  Reserved   _P(0x107)
458: #define  FADDR   _LP(0x108)
459: #define  FADDRHi _P(0x108)
460: #define  FADDRLo _P(0x109)
461: #define  FDATA   _P(0x10A)
462: #define  FDATAHi _P(0x10A)
463: #define  FDATALo _P(0x10B)
464: //#define  Reserved   _P(0x10C)
465: //#define  Reserved   _P(0x10D)
466: //#define  Reserved   _P(0x10E)
467: //#define  Reserved   _P(0x10F)
468:
469:
470: #define  ECLKDIV   _P(0x110)
471: //#define  Reserved   _P(0x111)
472: //#define  Reserved   _P(0x112)
473: #define  ECNFG   _P(0x113)
474: #define  EPROT   _P(0x114)
475: #define  ESTAT   _P(0x115)
476: #define  ECMD   _P(0x116)
477: //#define  Reserved   _P(0x117)
478: #define  EADDR   _LP(0x118)
479: #define  EADDRHi _P(0x118)
480: #define  EADDRLo _P(0x119)
```

```
481: #define  EDATA   _P(0x11A)
482: #define  EDATAHi _P(0x11A)
483: #define  EDATALo _P(0x11B)
484:
485:
486: //#define  Reserved   _P(0x11C)
487: //#define  Reserved   _P(0x11D)
488: //#define  Reserved   _P(0x11E)
489: //#define  Reserved   _P(0x11F)
490:
491:
492: #define  ATD1CTL0   _P(0x120)
493: #define  ATD1CTL01   _LP(0x120)
494: #define  ATD1CTL1   _P(0x121)
495: #define  ATD1CTL2   _P(0x122)
496: #define  ATD1CTL23   _LP(0x122)
497: #define  ATD1CTL3   _P(0x123)
498: #define  ATD1CTL4   _P(0x124)
499: #define  ATD1CTL45   _LP(0x124)
500: #define  ATD1CTL5   _P(0x125)
501: #define  ATD1STAT0   _P(0x126)
502: //#define  Reserved   _P(0x127)
503: #define  ATD1TEST01 _LP(0x128)
504: #define  ATD1TEST0 _P(0x128)
505: #define  ATD1TEST1 _P(0x129)
506: //#define  Reserved   _P(0x12A)
507: #define  ATD1STAT1   _P(0x12B)
508: //#define  Reserved   _P(0x12C)
509: #define  ATD1DIEN   _P(0x12D)
510: //#define  Reserved   _P(0x12E)
511: #define  PORTAD1   _P(0x12F)
512: #define  ATD1DR0   _LP(0x130)
513: #define  ATD1DR0H   _P(0x130)
514: #define  ATD1DR0L   _P(0x131)
515: #define  ATD1DR1   _LP(0x132)
516: #define  ATD1DR1H   _P(0x132)
517: #define  ATD1DR1L   _P(0x133)
518: #define  ATD1DR2   _LP(0x134)
519: #define  ATD1DR2H   _P(0x134)
520: #define  ATD1DR2L   _P(0x135)
521: #define  ATD1DR3   _LP(0x136)
522: #define  ATD1DR3H   _P(0x136)
523: #define  ATD1DR3L   _P(0x137)
524: #define  ATD1DR4   _LP(0x138)
525: #define  ATD1DR4H   _P(0x138)
526: #define  ATD1DR4L   _P(0x139)
527: #define  ATD1DR5   _LP(0x13A)
528: #define  ATD1DR5H   _P(0x13A)
529: #define  ATD1DR5L   _P(0x13B)
530: #define  ATD1DR6   _LP(0x13C)
531: #define  ATD1DR6H   _P(0x13C)
532: #define  ATD1DR6L   _P(0x13D)
533: #define  ATD1DR7   _LP(0x13E)
534: #define  ATD1DR7H   _P(0x13E)
535: #define  ATD1DR7L   _P(0x13F)
536:
537:
538:
539: #define  CAN0CTL01   _LP(0x140)
540: #define  CAN0CTL0   _P(0x140)
```

```
541: #define  CAN0CTL1   _P(0x141)
542: #define  CAN0BTR01   _LP(0x142)
543: #define  CAN0BTR0   _P(0x142)
544: #define  CAN0BTR1   _P(0x143)
545: #define  CAN0RFLG   _P(0x144)
546: #define  CAN0RIER   _P(0x145)
547: #define  CAN0TFLG   _P(0x146)
548: #define  CAN0TIER   _P(0x147)
549: #define  CAN0TARQ   _P(0x148)
550: #define  CAN0TAAK   _P(0x149)
551: #define  CAN0TBSEL   _P(0x14A)
552: #define  CAN0IDAC   _P(0x14B)
553: //#define  Reserved   _P(0x14C)
554: //#define  Reserved   _P(0x14D)
555: #define  CAN0RXERR   _P(0x14E)
556: #define  CAN0TXERR   _P(0x14F)
557: #define  CAN0IDAR0   _P(0x150)
558: #define  CAN0IDAR1   _P(0x151)
559: #define  CAN0IDAR2   _P(0x152)
560: #define  CAN0IDAR3   _P(0x153)
561: #define  CAN0IDMR0   _P(0x154)
562: #define  CAN0IDMR1   _P(0x155)
563: #define  CAN0IDMR2   _P(0x156)
564: #define  CAN0IDMR3   _P(0x157)
565: #define  CAN0IDAR4   _P(0x158)
566: #define  CAN0IDAR5   _P(0x159)
567: #define  CAN0IDAR6   _P(0x15A)
568: #define  CAN0IDAR7   _P(0x15B)
569: #define  CAN0IDMR4   _P(0x15C)
570: #define  CAN0IDMR5   _P(0x15D)
571: #define  CAN0IDMR6   _P(0x15E)
572: #define  CAN0IDMR7   _P(0x15F)
573:
574: #define  CAN0RXFG     _ADDR(0x160)
575: #define  CAN0RXIDR0   _P(0x160)
576: #define  CAN0RXIDR1   _P(0x161)
577: #define  CAN0RXIDR2   _P(0x162)
578: #define  CAN0RXIDR3   _P(0x163)
579: #define  CAN0RXDSR0   _P(0x164)
580: #define  CAN0RXDSR1   _P(0x165)
581: #define  CAN0RXDSR2   _P(0x166)
582: #define  CAN0RXDSR3   _P(0x167)
583: #define  CAN0RXDSR4   _P(0x168)
584: #define  CAN0RXDSR5   _P(0x169)
585: #define  CAN0RXDSR6   _P(0x16A)
586: #define  CAN0RXDSR7   _P(0x16B)
587: #define  CAN0RXDLR    _P(0x16C)
588:
589: #define  CAN0TXFG     _ADDR(0x170)
590: #define  CAN0TXIDR0   _P(0x170)
591: #define  CAN0TXIDR1   _P(0x171)
592: #define  CAN0TXIDR2   _P(0x172)
593: #define  CAN0TXIDR3   _P(0x173)
594: #define  CAN0TXDSR0   _P(0x174)
595: #define  CAN0TXDSR1   _P(0x175)
596: #define  CAN0TXDSR2   _P(0x176)
597: #define  CAN0TXDSR3   _P(0x177)
598: #define  CAN0TXDSR4   _P(0x178)
599: #define  CAN0TXDSR5   _P(0x179)
600: #define  CAN0TXDSR6   _P(0x17A)
```

```
601: #define  CAN0TXDSR7   _P(0x17B)
602: #define  CAN0TXDLR    _P(0x17C)
603: #define  CAN0TXTBPR    _P(0x17F)
604:
605:
606: #define  CAN1CTL0   _P(0x180)
607: #define  CAN1CTL1   _P(0x181)
608: #define  CAN1BTR0   _P(0x182)
609: #define  CAN1BTR1   _P(0x183)
610: #define  CAN1RFLG   _P(0x184)
611: #define  CAN1RIER   _P(0x185)
612: #define  CAN1TFLG   _P(0x186)
613: #define  CAN1TIER   _P(0x187)
614: #define  CAN1TARQ   _P(0x188)
615: #define  CAN1TAAK   _P(0x189)
616: #define  CAN1TBSEL   _P(0x18A)
617: #define  CAN1IDAC   _P(0x18B)
618: //#define  Reserved   _P(0x18C)
619: //#define  Reserved   _P(0x18D)
620: #define  CAN1RXERR   _P(0x18E)
621: #define  CAN1TXERR   _P(0x18F)
622: #define  CAN1IDAR0   _P(0x190)
623: #define  CAN1IDAR1   _P(0x191)
624: #define  CAN1IDAR2   _P(0x192)
625: #define  CAN1IDAR3   _P(0x193)
626: #define  CAN1IDMR0   _P(0x194)
627: #define  CAN1IDMR1   _P(0x195)
628: #define  CAN1IDMR2   _P(0x196)
629: #define  CAN1IDMR3   _P(0x197)
630: #define  CAN1IDAR4   _P(0x198)
631: #define  CAN1IDAR5   _P(0x199)
632: #define  CAN1IDAR6   _P(0x19A)
633: #define  CAN1IDAR7   _P(0x19B)
634: #define  CAN1IDMR4   _P(0x19C)
635: #define  CAN1IDMR5   _P(0x19D)
636: #define  CAN1IDMR6   _P(0x19E)
637: #define  CAN1IDMR7   _P(0x19F)
638:
639: #define  CAN1RXFG     _ADDR(0x160)
640: #define  CAN1RXIDR0   _P(0x1A0)
641: #define  CAN1RXIDR1   _P(0x1A1)
642: #define  CAN1RXIDR2   _P(0x1A2)
643: #define  CAN1RXIDR3   _P(0x1A3)
644: #define  CAN1RXDSR0   _P(0x1A4)
645: #define  CAN1RXDSR1   _P(0x1A5)
646: #define  CAN1RXDSR2   _P(0x1A6)
647: #define  CAN1RXDSR3   _P(0x1A7)
648: #define  CAN1RXDSR4   _P(0x1A8)
649: #define  CAN1RXDSR5   _P(0x1A9)
650: #define  CAN1RXDSR6   _P(0x1AA)
651: #define  CAN1RXDSR7   _P(0x1AB)
652: #define  CAN1RXDLR   _P(0x1AC)
653:
654: #define  CAN1TXFG     _ADDR(0x1B0)
655: #define  CAN1TXIDR0   _P(0x1B0)
656: #define  CAN1TXIDR1   _P(0x1B1)
657: #define  CAN1TXIDR2   _P(0x1B2)
658: #define  CAN1TXIDR3   _P(0x1B3)
659: #define  CAN1TXDSR0   _P(0x1B4)
660: #define  CAN1TXDSR1   _P(0x1B5)
```

```
661: #define  CAN1TXDSR2   _P(0x1B6)
662: #define  CAN1TXDSR3   _P(0x1B7)
663: #define  CAN1TXDSR4   _P(0x1B8)
664: #define  CAN1TXDSR5   _P(0x1B9)
665: #define  CAN1TXDSR6   _P(0x1BA)
666: #define  CAN1TXDSR7   _P(0x1BB)
667: #define  CAN1TXDLR   _P(0x1BC)
668: #define  CAN1TXTBPR   _P(0x1BF)
669:
670:
671: #define  CAN2CTL0   _P(0x1C0)
672: #define  CAN2CTL1   _P(0x1C1)
673: #define  CAN2BTR0   _P(0x1C2)
674: #define  CAN2BTR1   _P(0x1C3)
675: #define  CAN2RFLG   _P(0x1C4)
676: #define  CAN2RIER   _P(0x1C5)
677: #define  CAN2TFLG   _P(0x1C6)
678: #define  CAN2TIER   _P(0x1C7)
679: #define  CAN2TARQ   _P(0x1C8)
680: #define  CAN2TAAK   _P(0x1C9)
681: #define  CAN2TBSEL   _P(0x1CA)
682: #define  CAN2IDAC   _P(0x1CB)
683: //#define  Reserved   _P(0x1CC)
684: //#define  Reserved   _P(0x1CD)
685: #define  CAN2RXERR   _P(0x1CE)
686: #define  CAN2TXERR   _P(0x1CF)
687: #define  CAN2IDAR0   _P(0x1D0)
688: #define  CAN2IDAR1   _P(0x1D1)
689: #define  CAN2IDAR2   _P(0x1D2)
690: #define  CAN2IDAR3   _P(0x1D3)
691: #define  CAN2IDMR0   _P(0x1D4)
692: #define  CAN2IDMR1   _P(0x1D5)
693: #define  CAN2IDMR2   _P(0x1D6)
694: #define  CAN2IDMR3   _P(0x1D7)
695: #define  CAN2IDAR4   _P(0x1D8)
696: #define  CAN2IDAR5   _P(0x1D9)
697: #define  CAN2IDAR6   _P(0x1DA)
698: #define  CAN2IDAR7   _P(0x1DB)
699: #define  CAN2IDMR4   _P(0x1DC)
700: #define  CAN2IDMR5   _P(0x1DD)
701: #define  CAN2IDMR6   _P(0x1DE)
702: #define  CAN2IDMR7   _P(0x1DF)
703:
704: #define  CAN2RXFG     _ADDR(0x1E0)
705: #define  CAN2RXIDR0   _P(0x1E0)
706: #define  CAN2RXIDR1   _P(0x1E1)
707: #define  CAN2RXIDR2   _P(0x1E2)
708: #define  CAN2RXIDR3   _P(0x1E3)
709: #define  CAN2RXDSR0   _P(0x1E4)
710: #define  CAN2RXDSR1   _P(0x1E5)
711: #define  CAN2RXDSR2   _P(0x1E6)
712: #define  CAN2RXDSR3   _P(0x1E7)
713: #define  CAN2RXDSR4   _P(0x1E8)
714: #define  CAN2RXDSR5   _P(0x1E9)
715: #define  CAN2RXDSR6   _P(0x1EA)
716: #define  CAN2RXDSR7   _P(0x1EB)
717: #define  CAN2RXDLR   _P(0x1EC)
718:
719: #define  CAN2TXFG     _ADDR(0x1F0)
720: #define  CAN2TXIDR0   _P(0x1F0)
```

```
721: #define  CAN2TXIDR1   _P(0x1F1)
722: #define  CAN2TXIDR2   _P(0x1F2)
723: #define  CAN2TXIDR3   _P(0x1F3)
724: #define  CAN2TXDSR0   _P(0x1F4)
725: #define  CAN2TXDSR1   _P(0x1F5)
726: #define  CAN2TXDSR2   _P(0x1F6)
727: #define  CAN2TXDSR3   _P(0x1F7)
728: #define  CAN2TXDSR4   _P(0x1F8)
729: #define  CAN2TXDSR5   _P(0x1F9)
730: #define  CAN2TXDSR6   _P(0x1FA)
731: #define  CAN2TXDSR7   _P(0x1FB)
732: #define  CAN2TXDLR   _P(0x1FC)
733: #define  CAN2TXTBPR   _P(0x1FF)
734:
735:
736: #define  CAN3CTL0   _P(0x200)
737: #define  CAN3CTL1   _P(0x201)
738: #define  CAN3BTR0   _P(0x202)
739: #define  CAN3BTR1   _P(0x203)
740: #define  CAN3RFLG   _P(0x204)
741: #define  CAN3RIER   _P(0x205)
742: #define  CAN3TFLG   _P(0x206)
743: #define  CAN3TIER   _P(0x207)
744: #define  CAN3TARQ   _P(0x208)
745: #define  CAN3TAAK   _P(0x209)
746: #define  CAN3TBSEL   _P(0x20A)
747: #define  CAN3IDAC   _P(0x20B)
748: //#define  Reserved   _P(0x20C)
749: //#define  Reserved   _P(0x20D)
750: #define  CAN3RXERR   _P(0x20E)
751: #define  CAN3TXERR   _P(0x20F)
752: #define  CAN3IDAR0   _P(0x210)
753: #define  CAN3IDAR1   _P(0x211)
754: #define  CAN3IDAR2   _P(0x212)
755: #define  CAN3IDAR3   _P(0x213)
756: #define  CAN3IDMR0   _P(0x214)
757: #define  CAN3IDMR1   _P(0x215)
758: #define  CAN3IDMR2   _P(0x216)
759: #define  CAN3IDMR3   _P(0x217)
760: #define  CAN3IDAR4   _P(0x218)
761: #define  CAN3IDAR5   _P(0x219)
762: #define  CAN3IDAR6   _P(0x21A)
763: #define  CAN3IDAR7   _P(0x21B)
764: #define  CAN3IDMR4   _P(0x21C)
765: #define  CAN3IDMR5   _P(0x21D)
766: #define  CAN3IDMR6   _P(0x21E)
767: #define  CAN3IDMR7   _P(0x21F)
768:
769: #define  CAN3RXFG     _ADDR(0x220)
770: #define  CAN3RXIDR0   _P(0x220)
771: #define  CAN3RXIDR1   _P(0x221)
772: #define  CAN3RXIDR2   _P(0x222)
773: #define  CAN3RXIDR3   _P(0x223)
774: #define  CAN3RXDSR0   _P(0x224)
775: #define  CAN3RXDSR1   _P(0x225)
776: #define  CAN3RXDSR2   _P(0x226)
777: #define  CAN3RXDSR3   _P(0x227)
778: #define  CAN3RXDSR4   _P(0x228)
779: #define  CAN3RXDSR5   _P(0x229)
780: #define  CAN3RXDSR6   _P(0x22A)
```

```
781: #define  CAN3RXDSR7   _P(0x22B)
782: #define  CAN3RXDLR   _P(0x22C)
783:
784: #define  CAN3TXFG     _ADDR(0x230)
785: #define  CAN3TXIDR0   _P(0x230)
786: #define  CAN3TXIDR1   _P(0x231)
787: #define  CAN3TXIDR2   _P(0x232)
788: #define  CAN3TXIDR3   _P(0x233)
789: #define  CAN3TXDSR0   _P(0x234)
790: #define  CAN3TXDSR1   _P(0x235)
791: #define  CAN3TXDSR2   _P(0x236)
792: #define  CAN3TXDSR3   _P(0x237)
793: #define  CAN3TXDSR4   _P(0x238)
794: #define  CAN3TXDSR5   _P(0x239)
795: #define  CAN3TXDSR6   _P(0x23A)
796: #define  CAN3TXDSR7   _P(0x23B)
797: #define  CAN3TXDLR   _P(0x23C)
798: #define  CAN3TXTBPR   _P(0x23F)
799:
800:
801:
802: #define  PTT   _P(0x240)
803: #define  PTIT   _P(0x241)
804: #define  DDRT   _P(0x242)
805: #define  RDRT   _P(0x243)
806: #define  PERT   _P(0x244)
807: #define  PPST   _P(0x245)
808: //#define  Reserved   _P(0x246)
809: //#define  Reserved   _P(0x247)
810: #define  PTS   _P(0x248)
811: #define  PTIS   _P(0x249)
812: #define  DDRS   _P(0x24A)
813: #define  RDRS   _P(0x24B)
814: #define  PERS   _P(0x24C)
815: #define  PPSS   _P(0x24D)
816: #define  WOMS   _P(0x24E)
817: //#define  Reserved   _P(0x24F)
818:
819: #define  PTM   _P(0x250)
820: #define  PTIM   _P(0x251)
821: #define  DDRM   _P(0x252)
822: #define  RDRM   _P(0x253)
823: #define  PERM   _P(0x254)
824: #define  PPSM   _P(0x255)
825: #define  WOMM   _P(0x256)
826: #define  MODRR   _P(0x257)
827: #define  PTP   _P(0x258)
828: #define  PTIP   _P(0x259)
829: #define  DDRP   _P(0x25A)
830: #define  RDRP   _P(0x25B)
831: #define  PERP   _P(0x25C)
832: #define  PPSP   _P(0x25D)
833: #define  PIEP   _P(0x25E)
834: #define  PIFP   _P(0x25F)
835: #define  PTH   _P(0x260)
836: #define  PTIH   _P(0x261)
837: #define  DDRH   _P(0x262)
838: #define  RDRH   _P(0x263)
839: #define  PERH   _P(0x264)
840: #define  PPSH   _P(0x265)
```

```
841: #define  PIEH   _P(0x266)
842: #define  PIFH   _P(0x267)
843: #define  PTJ   _P(0x268)
844: #define  PTIJ   _P(0x269)
845: #define  DDRJ   _P(0x26A)
846: #define  RDRJ   _P(0x26B)
847: #define  PERJ   _P(0x26C)
848: #define  PPSJ   _P(0x26D)
849: #define  PIEJ   _P(0x26E)
850: #define  PIFJ   _P(0x26F)
851:
852: //#define  Reserved   _P(0x270 - 0x27F)
853:
854:
855: #define  CAN4CTL0   _P(0x280)
856: #define  CAN4CTL1   _P(0x281)
857: #define  CAN4BTR0   _P(0x282)
858: #define  CAN4BTR1   _P(0x283)
859: #define  CAN4RFLG   _P(0x284)
860: #define  CAN4RIER   _P(0x285)
861: #define  CAN4TFLG   _P(0x286)
862: #define  CAN4TIER   _P(0x287)
863: #define  CAN4TARQ   _P(0x288)
864: #define  CAN4TAAK   _P(0x289)
865: #define  CAN4TBSEL   _P(0x28A)
866: #define  CAN4IDAC   _P(0x28B)
867: //#define  Reserved   _P(0x28C)
868: //#define  Reserved   _P(0x28D)
869: #define  CAN4RXERR   _P(0x28E)
870: #define  CAN4TXERR   _P(0x28F)
871:
872:
873: #define  CAN4IDAR0   _P(0x290)
874: #define  CAN4IDAR1   _P(0x291)
875: #define  CAN4IDAR2   _P(0x292)
876: #define  CAN4IDAR3   _P(0x293)
877: #define  CAN4IDMR0   _P(0x294)
878: #define  CAN4IDMR1   _P(0x295)
879: #define  CAN4IDMR2   _P(0x296)
880: #define  CAN4IDMR3   _P(0x297)
881: #define  CAN4IDAR4   _P(0x298)
882: #define  CAN4IDAR5   _P(0x299)
883: #define  CAN4IDAR6   _P(0x29A)
884: #define  CAN4IDAR7   _P(0x29B)
885: #define  CAN4IDMR4   _P(0x29C)
886: #define  CAN4IDMR5   _P(0x29D)
887: #define  CAN4IDMR6   _P(0x29E)
888: #define  CAN4IDMR7   _P(0x29F)
889:
890: #define  CAN4RXFG     _ADDR(0x2A0)
891: #define  CAN4RXIDR0   _P(0x2A0)
892: #define  CAN4RXIDR1   _P(0x2A1)
893: #define  CAN4RXIDR2   _P(0x2A2)
894: #define  CAN4RXIDR3   _P(0x2A3)
895: #define  CAN4RXDSR0   _P(0x2A4)
896: #define  CAN4RXDSR1   _P(0x2A5)
897: #define  CAN4RXDSR2   _P(0x2A6)
898: #define  CAN4RXDSR3   _P(0x2A7)
899: #define  CAN4RXDSR4   _P(0x2A8)
900: #define  CAN4RXDSR5   _P(0x2A9)
```

```
901: #define  CAN4RXDSR6   _P(0x2AA)
902: #define  CAN4RXDSR7   _P(0x2AB)
903: #define  CAN4RXDLR   _P(0x2AC)
904:
905: #define  CAN4TXFG     _ADDR(0x2B0)
906: #define  CAN4TXIDR0   _P(0x2B0)
907: #define  CAN4TXIDR1   _P(0x2B1)
908: #define  CAN4TXIDR2   _P(0x2B2)
909: #define  CAN4TXIDR3   _P(0x2B3)
910: #define  CAN4TXDSR0   _P(0x2B4)
911: #define  CAN4TXDSR1   _P(0x2B5)
912: #define  CAN4TXDSR2   _P(0x2B6)
913: #define  CAN4TXDSR3   _P(0x2B7)
914: #define  CAN4TXDSR4   _P(0x2B8)
915: #define  CAN4TXDSR5   _P(0x2B9)
916: #define  CAN4TXDSR6   _P(0x2BA)
917: #define  CAN4TXDSR7   _P(0x2BB)
918: #define  CAN4TXDLR   _P(0x2BC)
919: #define  CAN4TXTBPR   _P(0x2BF)
920:
921:
922: //#define  Reserved   _P(0x2C0 - 0x3FF)
923:
924:
925: #define  BDMSTS   _P(0xFF01)
926: #define  BDMCCR   _P(0xFF06)
927: #define  BDMINR   _P(0xFF07)
928:
929: #endif
930:
```